Abstract—Cognitive radio has been put forward to make efficient use of scarce radio frequency spectrum. Spectrum sensing is the cornerstone of cognitive radio. As a part of the effort toward building a cognitive radio network testbed, we have demonstrated real-time spectrum sensing [1]. However, current hardware platforms for cognitive radio introduce time delays that actually undermine the accuracy of spectrum sensing. The time delay, named response delay, incurred by hardware and software can be measured at the receiving antenna and the transmitting antenna co-located at a secondary user (SU). In this paper, minimum response delays are experimentally quantified and reported based on two hardware platforms, the universal software radio peripheral 2 (USRP2) and the small form factor software defined radio development platform (SFF SDR DP). In a subsequent paper, an approach for single-user prediction is proposed to combat with the response delays. This work is a part of the effort toward building a cognitive radio network testbed.

I. INTRODUCTION

Cognitive radio (CR) has been viewed as a promising technology to make efficient use of the radio frequency spectrum. It introduces “intelligence” to traditional radios. Spectrum sensing is the cornerstone of CR, which detects the availability of the radio frequency spectrum for secondary user (SU). The effectiveness of spectrum sensing has strong impact on the spectrum utilization of CR.

A number of spectrum sensing techniques have been proposed, such as energy detection, matched filter detection, cyclostationary feature detection, covariance-based detection, and wavelet-based detection [2], [3], [4], [5], [6].

In addition to tremendous efforts on theoretical investigations, work on hardware implementation of spectrum sensing has been reported as well in [7], [8], [9], [10]. Experience gained in developing software defined radio (SDR) can benefit CR work, and existing SDR development platforms can be extended for developing CR transceivers. More recently, real-time spectrum sensing on hardware platform with controllable primary users has been demonstrated in [1].

Implementing effective spectrum sensing schemes is a fundamental part of development effort toward a cognitive radio network testbed [11], [12]. It is worth noting that measurement can be critical in guiding implementation work and verifying algorithm performance. In implementing the algorithms on hardware platforms, we have found, however, time delay introduced by hardware platforms becomes non-negligible, though in theoretical investigations such time delay is usually ignored. Accurately quantifying this delay is necessary since it is wise to take into account the measured results in algorithm design and implementation.

There have been some hardware platforms that can be used for CR, such as the universal software radio peripheral (USRP), the universal software radio peripheral 2 (USRP2) [13], the small form factor software defined radio development platform (SFF SDR DP) [14], the wireless open-access research platform (WARP) [15], the Sora [16], and so on.

There exist a few studies on discussions of the time delay of the USRP platform. In [17], the time delay between the GNU Radio [18] and the field-programmable gate array (FPGA) is reported. The value ranges from 289 us to 9 ms. In [19], an elapsed time is measured, where the elapsed time is the length from the start time of sending out a data link control (DLC) frame to the instance of completely receiving an acknowledgment DLC frame of the same size. The average of the time is 3.14 ms. In [20], the measured receive latency ranges from 1 ms to 30 ms, and the transmit latency ranges from 28.9 ms to 36.9 ms.

The measured time delays of USRP differ so much. One reason is that what are reported are different portions of the time delay. We have not seen any reported measured time delays of the USRP2 platform and the SFF SDR DP.

The contributions of this paper are summarized as follows. First, the problem of response delay is formulated. Second, the minimum response delays of the USRP2 platform and the SFF SDR DP are measured and reported.

The rest of this paper is organized as follows. Section II formulates the problem. Section III reports the measurements of the minimum response delays of the USRP2 platform and the SFF SDR DP. And Section IV concludes this paper.

II. PROBLEM FORMULATION

In this section, a scenario of spectrum sensing is described. The time slot and the response delay are introduced.

A. Time Slot Structure

Consider a scenario shown in Fig. 1, where an SU communicates with another SU or a secondary base station (SBS) through wireless channels, and both uplink channel and downlink channel are comprised of a sequence of time
slots. Assume time slot level synchronization is performed and the length of the time slots is constant. Each time slot contains two phases: spectrum sensing phase (the first phase) and communication phase (the second phase). In the spectrum sensing phase of a time slot, a potential SU sender or SBS sender senses the availability of the channel, then it may start data transmission in the following communication phase if the sensed channel state is “idle”.

In order to verify the sensed channel states, the actual channel states are required. How can SUs get the actual channel states without the aids of PUs? Consider the two cases: (1) the sensed channel state is “idle”, so the SU sender can (1a) send data in the next communication phase, or (1b) hold on data transmission in the next communication phase, and (2) the sensed channel state is “busy”, so the SU sender holds on data transmission in the next communication phase. In [21], acknowledgment (ACK) and negative acknowledgment (NAK) messages are employed to indicate whether a transmission is successful or not. The same idea is borrowed here for case (1a) verification. As shown in Fig. 1, ACK or NAK messages are sent from the targeted receiver to the sender together with other kinds of data in the communication phase. Take an uplink data transmission as an example, if an SU sender receives an ACK (or NAK) message from the targeted SU receiver, it means the uplink data transmitted in the particular time slot have been received successfully (or unsuccessfully), which confirms the uplink in that time slot is “idle” (or “busy”). Note that the verification process introduces a time delay contributed by propagation and signal processing. On the other hand, for case (1b) and case (2) verification, it is assumed that the SU sender is able to verify the channel state by itself using the signals received in the following communication phase.

B. Response Delay

To explain the response delay, a simplified data path of SU is shown in Fig. 2. Received radio frequency (RF) signals are filtered, amplified, down-converted and digitized by an analog-to-digital converter (ADC). Then the digital signals are fed to a data processing module through a digital data interface, which ends the reception process. The transmission process starts with sending the digital data from the data processing module and ends at the transmitting antenna, through a data interface, a digital-to-analog converter (DAC) and an up-conversion module. Note that the down-conversion and the up-conversion modules are optional. For instance, in [22], down-conversion is employed, whereas in [12], wideband spectrum is measured directly without down-conversion. Also note that data interfaces and buffers on the data path may introduce delay.

The response delay is a delay as a cognitive radio device receives a signal from a channel over the air for spectrum sensing, then transmits data to the air using the channel if the channel is believed to be available. This delay is contributed by three sections partitioned by test points A, B, C and D (referring to Fig. 2 and Fig. 3). The corresponding delays are denoted by $t_{rl}$, $t_{pl}$, and $t_{tl}$, respectively. Then the total time delay $t_t$ or response delay is:

$$ t_t = t_{rl} + t_{pl} + t_{tl} \tag{1} $$

The response delay can vary depending on how heavy the data processing is. The minimum response delay refers to the response delay with minimum processing work, i.e., loopback (just passing through data without actual processing), in the data processing module.
Fig. 4. Setup for the measurement of the response delay of USRP2.

If the response delay $t_i$ is comparable with or greater than the length of a time slot, it cannot be ignored. Fig. 3 shows a special case that the response delay equals to the length of a time slot. In this case, if an SU detects the channel state to be “idle” during the spectrum sensing phase of time slot 0, it may start a data transmission immediately. However, the actual data transmission over the air happens during the communication phase of time slot 1. Since the channel state may change in one time slot, the data transmission of the SU can interfere PUs during time slot 1. In order to minimize such negative impacts caused by the response delay, prediction of channel state is proposed in this paper. Obviously, the response delay leads to a reduced correlation between current spectrum sensing phase and next targeted communication phase(s). Achieving accurate prediction at least $t_i$ ahead can be very challenging.

We are building a cognitive radio network testbed with tens of nodes at Tennessee Technological University to demonstrate the concept of cognitive radio networks and dig out more problems from the aspect of system for future research. Response delay is the first problem we met. Such delay is inherent in many off-the-shelf hardware platforms for cognitive radio, as demonstrated in Section III.

III. MEASUREMENT OF MINIMUM RESPONSE DELAY

As mentioned above, hardware platforms for cognitive radio introduce unwanted time delays, but how long are they? What are the minimum response delays? These can be answered using measurements reported below.

Two candidates are chosen from existing commercial hardware platforms that can be used for cognitive radio. One is the USRP2, which uses an architecture of host-based processing. In this architecture, RF front-end and data conversion modules are co-located on external boards, and the converted digital data is transferred to a host computer for further processing. The other one is the SFF SDR DP, which uses a stand-alone architecture and is able to handle all the signal processing on its boards.

Fig. 4 and Fig. 5 show the measurement setups for the two platforms. Basically, the way is to feed a signal to the receiving antenna and check the time delay at the transmitting antenna. An arbitrary waveform generator (AWG), Tektronix AWG7122B, generates a sequence of gated sinusoidal waveforms of 250 MHz. The sinusoidal burst lasts 50 $\mu$s (for the measurement of USRP2) or 500 $\mu$s (for the measurement of SFF SDR DP), and the burst appears once every 2 seconds. We have found the duty cycle of 2 seconds is sufficient since none of the minimum response delays exceeds 2 seconds.

The output of the AWG is connected with both the receiving antenna port and a digital phosphor oscilloscope (DPO), Tektronix DPO72004, using two subminiature version A (SMA) cables through a power divider PE2068. The transmitting antenna port is also connected with the DPO using an SMA cable. The DPO is employed to display the signals at both the receiving antenna port and the transmitting antenna port on the same screen, so that the response delay can be read out. The DPO supports a maximum bandwidth of 20 GHz and a maximum sampling rate of 50 GS/s. It has four channels and the ability of recording 250 M samples per channel. The AWG supports a maximum sampling rate of 12 GS/s. It has two channels and is able to store 64 M samples for each channel.

The USRP2 consists of a motherboard and one or more selectable RF daughterboards [13]. The major computing power on the motherboard comes from a Xilinx Spartan-3 XC3S2000 FPGA. The motherboard is also equipped with a 100 MS/s 14-bit dual-channel ADC, a 400 MS/s 16-bit dual-channel DAC, and a Gigabit Ethernet port for connecting to a host computer. Among the RF daughterboards available for USRP2 there is a newly developed one called WBX that covers a wide frequency range of 50 MHz to 2.2 GHz, with a nominal noise figure of 5-7 dB. In the measurement of the minimum response delay of USRP2, a USRP2 motherboard with the WBX RF daughterboard is connected directly to a host laptop computer via the Gigabit Ethernet. The GNU Radio companion (GRC) runs on the host computer with Linux operating system. Using the GRC, a USRP2 source block and a USRP2 sink block are connected directly to form a loopback configuration.

500 consecutive readouts of the minimum response delay of USRP2 are recorded. Fig. 6 shows one readout on the DPO. Fig. 7 shows the distribution of the measured minimum response delays that spread from about 2 ms to about 16 ms. Random minimum response delays of USRP2 are observed, which is not surprising since both the Ethernet and the computer operating system can introduce randomness.
The SFF SDR DP consists of three separate boards: digital processing module, data conversion module, and RF module [14]. The digital processing module is designed based on the TMS320DM6446 system-on-chip (SoC) from Texas Instruments (TI) and the Virtex-4 SX35 FPGA from Xilinx. The TMS320DM6446 SoC has a C64x+ digital signal processor (DSP) core running at 594 MHz together with an advanced RISC machine 9 (ARM9) core running at 297 MHz. The digital processing module also comes with a 10/100 Mbps Ethernet port. The data conversion module is equipped with a 125 MS/s 14-bit dual-channel ADC, a 500 MS/s 16-bit dual-channel DAC, as well as a Xilinx Virtex-4 LX25 FPGA. The low-band tunable RF module employed in this measurement can be configured to have either a 5 MHz or a 20 MHz bandwidth with working frequencies of 200-1050 MHz for the transmitter and 200-1000 MHz for the receiver. The nominal noise figure of this RF module is 5 dB.

In the minimum response delay measurement for SFF SDR DP, an example project called SFF_SDR_RF_Loopback_ADACIII coming with the Lyrtech software package runs on both the FPGA and the DSP on the digital processing module. The function TASK_Transmit for the DSP in the example project is slightly modified to simply loop back all the received data. 100 consecutive readouts of the minimum response delay of SFF SDR DP are recorded. All the readout values are unanimously around 48 ms. Fig. 8 shows one readout on the DPO. Although it is a little surprising to observe that the minimum response delay of SFF SDR DP is larger than that of USRP2, its constant minimum time delay is a desired feature for system design. A larger minimum response delay may be contributed by the interfaces and data buffers on the data path.

From these measurements one can see the minimum response delays can be up to tens of milliseconds. The minimum response delays are measured without performing sophisticated base-band processing. In practice, additional time delay will be added on the top of the minimum response delay. The total response delay and the uncertainty range have to be considered in the CR system design.

IV. CONCLUSION

The response delay issue has been identified. Moreover, the minimum response delays of two hardware platforms that can be used for cognitive radio have been measured. The measurement results can guide our future work in developing the cognitive radio network testbed.

In a subsequent paper, an approach for single-user prediction of channel state is proposed to boost the accuracy of spectrum sensing and minimize the negative impact of the response delays caused by hardware platforms.

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