Building A Cognitive Radio Network Testbed

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Outline

- Introduction
- Off-the-Shelf Hardware Platforms for Cognitive Radio Networks
- Proposed Cognitive Radio Network Testbed
- Conclusion
Traffic

- Wireless channels can be viewed as lanes of highway.
  - Some highways are highly occupied…
  - Whereas some are nearly empty…
- One ideal solution: let the cars on highly occupied highways use less occupied highways.
- Applying this idea to wireless channels, we get the basic idea of cognitive radio!
Cognitive Radio

- Cognitive radio is viewed as a novel approach for improving the utilization of the precious radio spectrum.
- Cognitive Radio – a technique of utilizing unused spectrums to communicate efficiently for secondary users without interfering primary users. It is able to sense, to learn, and to adapt.
Overview

- A testbed for cognitive radio can not only verify concepts, algorithms, and protocols, but also dig out more practical problems for future research. To our best knowledge, an authentic real-time cognitive radio system has never been demonstrated.

- In order to build a cognitive radio network testbed, four popular commercial off-the-shelf hardware platforms are investigated. Unfortunately, none of them meets our needs.

- In this paper, an architecture of the motherboard and a functional architecture for the nodes of cognitive radio network testbeds, and an architecture for cognitive radio network testbeds, are proposed.
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There exist some commercial off-the-shelf hardware platforms designed for software defined radio (SDR) that could be used for building the nodes of cognitive radio networks.

- Universal Software Radio Peripheral 2 (USRP2)
- Small-Form-Factor Software-Defined-Radio Development Platform (SFF SDR DP)
- Wireless Open-Access Research Platform (WARP)
- Microsoft Research Software Radio (Sora)
Universal Software Radio Peripheral 2 (USRP2)

- Xilinx Spartan-3 FPGA
- 100 MS/s 14-bit dual channel ADC
- 400 MS/s 16-bit dual channel DAC
- WBX RF daughterboard
  - 50 MHz – 2.2 GHz
- Gigabit Ethernet

Host-based
Universal Software Radio Peripheral 2 (USRP2)

- **Advantage**
  - USRP2 works with GNU Radio, which simplifies and eases the usage of USRP2.

- **Disadvantages**
  - Random time delays introduced by the Gigabit Ethernet and host computer operating system
  - USRP2 needs a powerful host computer.
Small-Form-Factor Software-Defined-Radio Development Platform (SFF SDR DP)

RF module:
- 5 MHz or 20 MHz bandwidth,
- 200-1050 MHz for the transmitter,
- 200-1000 MHz for the receiver

Data conversion module:
- 125 MS/s 14-bit dual channel ADC,
- 500 MS/s 16-bit dual channel DAC,
- Virtex-4 LX25 FPGA

Digital processing module:
- TMS320DM6446 (DSP+ARM9),
- Virtex-4 SX35 FPGA,
- 10/100 Mb/s Ethernet

Stand-alone
Small-Form-Factor Software-Defined-Radio Development Platform (SFF SDR DP)

Advantage
- SFF SDR DP is in small form factor and can be moved easily.
- It supports full-duplex communications.

Disadvantages
- Its computing capacity is fixed and it is not easy to upgrade to meet the needs of CRN testbeds.
- The minimum response delay is not trivial.
Wireless Open-Access Research Platform (WARP)

Xilinx Virtex-4 FX100 FPGA with PowerPC

Gigabit Ethernet

Radio board:
Dual-channel 65 MS/s 14-bit ADC,
Dual-channel 125 MS/s 16-bit DAC,
bandwidth up to 40 MHz,
covering 2400-2500 MHz
and 4900-5875 MHz
Wireless Open-Access Research Platform (WARP)

■ Advantage
  □ Stand-alone hardware platform
  □ Both physical layer and MAC layer can be implemented on one FPGA.

■ Disadvantages
  □ The FPGA on WARP is not powerful enough for cognitive radio networks.
Microsoft Research Software Radio (Sora)

Host-based

Radio control board (RCB):
Xilinx Virtex-5 FPGA, PCIe interface

RF board:
can be WARP radio board
Microsoft Research Software Radio (Sora)

■ Advantage
  □ High-throughput interface between the RF board and a host computer

■ Disadvantages
  □ The host computer has to be very powerful.
  □ Implementing real-time full-duplex communications on the host computer is challenging.
  □ The host computer installed with Sora lacks mobility.
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The Requirements

- To our best understanding, major concerns on hardware platforms for cognitive radio network testbeds are:
  - Computing power
  - Response time delay
- Cognitive radio requires much more computing powers than SDR.
- If the response time delay is large, the throughput of cognitive radio network testbeds will seriously degrade.
- Full-duplex communications is preferable.
- Unfortunately, none of the existing off-the-shelf hardware platforms can meet all of the above requirements.
The use of two FPGAs is a trade-off between performance and cost.
Proposed Functional Architecture for the Nodes
Proposed Cognitive Radio Network Testbed

- The console computer controls and coordinates all the nodes in the testbed.
- This testbed can also be used for other applications, such as smart grid and wireless tomography.
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Conclusion

■ Popular commercial off-the-shelf hardware platforms designed for software defined radio have been introduced and investigated.

■ In order to overcome the shortcomings of the off-the-shelf hardware platforms, an architecture of the motherboard and a functional architecture for the nodes of cognitive radio network testbeds, as well as an architecture for cognitive radio network testbeds, have been proposed.
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